PATENT ABSTRACTS OF JAPAN

(11)Publication number : **05-048460**
(43)Date of publication of application : **26.02.1993**

(51)Int.Cl. **H03M 1/46**
H03M 1/08
H03M 1/12
H04N 1/40
H04N 1/40

(21)Application number : **03-236059**
(22)Date of filing : **17.09.1991**

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(30)Priority
Priority number : **03133985** Priority date : **05.06.1991** Priority country : **JP**

(54) A/D CONVERTER AND SENSOR USING THE SAME AND THREE-DIMENSIONAL INTEGRATED CIRCUIT

(57)Abstract:
PURPOSE: To apply the A/D converter to a 3-dimensional integrated circuit and an array sensor by devising the A/D converter in such a way that plural analog signals inputted in parallel are converted into digital signals at a high speed with high accuracy.
CONSTITUTION: This A/D converter is provided with plural analog signal input terminals 1, an analog signal storage section 4, plural comparators 10, a single D/A converter 9, a digital counter 5, digital value storage sections 12, 14, 15, and a scanning circuit 16. The different analog signal fed to each analog signal input terminal 1 is stored in the analog quantity storage section 4 and inputted to a comparator 10 together with a reference output of the D/A converter 9 increasing gradually attended with the operation of the counter, the data of the counter when the reference output is higher than each inputted analog value is stored individually to a digital quantity storage section 4 and the data therein is read sequentially as a digital value by the scanning circuit 16.

LEGAL STATUS

[Date of request for examination]	14.01.1997
[Date of sending the examiner's decision of rejection]	26.06.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]

[Claim 1] Two or more analog value are recording sections which accumulate each analog data inputted from two or more analog data input terminal and two or more of these analog data input terminals, A digital counter and the D/A converter which changes the digitized output of this digital counter into an analog value, compared the output value and said analog data of this D/A converter, and when said digital counter was a rise counter, the output value of said D/A converter exceeded said analog data -- or Two or more comparison means to distinguish that the output value of said D/A converter was less than said analog data when said digital counter is a down counter, The A/D converter equipped with the digital value are recording section which memorizes the digital value of said D/A converter in response to control by two or more of these comparison means.

[Claim 2] The analog value are recording section which accumulates each analog data inputted from two or more analog data input terminal and two or more of these analog data input terminals, A digital counter and the D/A converter which changes the digitized output of this digital counter into an analog value, compared the output value and said analog data of this D/A converter, and when said digital counter was a rise counter, the output value of said D/A converter exceeded said analog data -- or Two or more comparison means to distinguish that the output value of said D/A converter was less than said analog data when said digital counter is a down counter, The A/D converter according to claim 1 which is an A/D converter equipped with the digital value are recording section which memorizes the digital value of said D/A converter in response to control by two or more of these comparison means, and was equipped with the scanning circuit which reads the output of the data of said digital value are recording section one by one further.

[Claim 3] The A/D converter [equipped with the transfer switch train which controls transfer of the digital value from the 2nd are recording section which transmits said digital value which memorized and memorized the digital value of a D/A converter based on two or more comparison means to the digital value are recording section, and this are recording section to the 2nd digital value are recording section] according to claim 2.
[Claim 4] The sensor of a digital signal output which connected the output of an array-like sensing component to the analog data input terminal of an A/D converter according to claim 2.
[Claim 5] The sensor [equipped with the optoelectric transducer which is a sensing component which made the shape of an array, the perpendicular charge transfer way of two or more trains, and the amplifier which transforms a charge into an electrical potential difference and makes this analog output] according to claim 4.
[Claim 6] The sensor equipped with the circuit which amplifies the electrical-potential-difference value output from two or more optoelectric transducers which made the shape of an array for every perpendicular output line in a follower circuit, and removes a fixed pattern noise for every train.
[Claim 7] Amplify the electrical-potential-difference value output from two or more optoelectric transducers which made the shape of an array in a follower circuit, and it outputs to each perpendicular output line. While connecting one terminal of joint capacity to each of this perpendicular output line, the other-end child of said joint capacity is connected to one terminal of a switch. Furthermore, it is the sensor which takes the configuration which connected the other end of said switch to the fixed potential line. Said switch is turned ON when the follower output which bears light exposure information has appeared in the perpendicular output line. By outputting the follower output of said transistor for magnification which resets the gate potential of the transistor for magnification and has gate potential in reset potential at said perpendicular output line after this switch turns off The sensor equipped with the circuit which outputs the electrical potential difference of the difference of the follower output of said transistor for magnification which has gate potential in reset potential, and the follower output which bore said light exposure information to said joint capacity terminal, and removes a fixed pattern noise for every perpendicular output line.
[Claim 8] The sensor [equipped with the circuit which gives the analog output which amplified the electrical-potential-difference value output from two or more optoelectric transducers which made the shape of an array in the follower circuit, and removed the fixed pattern noise for every train] according to claim 4.
[Claim 9] Amplify the electrical-potential-difference value output from two or more optoelectric transducers which made the shape of an array in a follower circuit, and it outputs to each perpendicular output line. While connecting one terminal of joint capacity to each of this perpendicular output line, the other-end child of said joint capacity is connected to one terminal of a switch. Furthermore, it is the sensor which takes the configuration which connected the other end of said switch to the fixed potential line. Said switch is turned ON when the follower output which bears light exposure information has appeared in the perpendicular output line. By outputting the follower output of said transistor for magnification which resets the gate potential of the transistor for magnification and has gate potential in reset potential at said perpendicular output line after this switch turns off The sensor [equipped with the circuit which outputs the

electrical potential difference of the difference of the follower output of said transistor for magnification which has gate potential in reset potential, and the follower output which bore said light exposure information to said joint capacity terminal, and removes a fixed pattern noise for every perpendicular output line] according to claim 4.
[Claim 10] The three-dimension integrated circuit of a configuration of having an A/D converter according to claim 1 as a component of an A/D-conversion layer, and inputting respectively two or more analog data from other layers into two or more analog data input terminals of said A/D converter.
[Claim 11] The three-dimension integrated circuit according to claim 10 characterized by changing the analog value output from an array-like sensing component into digital value at juxtaposition.
[Claim 12] The three-dimension integrated circuit according to claim 11 characterized by what impedance conversion of the terminal voltage of two or more photo-electric-conversion devices which change according to light exposure is carried out, and is transmitted to each A/D converter.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the sensor and three-dimension integrated circuit having the equipment which changes two or more analog values into digital value, and said inverter.
[0002]
[Description of the Prior Art] Although various things, such as an integral mold, a successive approximation type, and a flash plate mold, exist as equipment (it is described as an A/D converter below) which changes an analog value into digital value, neither changes one analog value into digital value serially in detail fundamentally, and does not change two or more analog values into coincidence. Moreover, in the case of the image sensors which have an A/D converter, the gestalt connects to one analog output terminal common to each pixel of image sensors the above A/D converters which have one input terminal fundamentally, and changes into digital value in detail the analog signal value outputted serially.
[0003]
[Problem(s) to be Solved by the Invention] The following technical problems exist in the A/D converter of the above-mentioned conventional example. That is, although the A/D converter of a flash plate mold can carry out high-speed conversion, a circuit complicates it by leaps and bounds with the rise of resolution, and a conversion rate is small [the A/D converter] although the A/D converter of an integral mold is highly precise. By the three-dimension integrated circuit which carries out signal processing of two or more analog value data organically, and the sensor of the shape of an array which obtains analog value data from two or more sensing components, in order to perform various data processing, it is necessary to carry out A/D conversion of the data of an analog value generally inputted. Especially the thing done for A/D conversion, without the effect of time amount,

a spike noise, etc. which the standup of an analog output wave takes becoming large in connection with high-speed read-out, therefore reducing the precision of a signal value although image sensors require read-out of high-speed image data increasingly in recent years from a viewpoint of the improvement in a manuscript reading rate and improvement in resolution becomes difficult. Moreover, it is necessary to change into digital value two or more analog values which distribute and exist in the interior inevitably in a three-dimension integrated circuit at a high speed. In this case, although it is possible at a high speed to carry out sequential conversion serially, carrying out a multiplexer about two or more above-mentioned analog values using the A/D converter of large 1 input of a circuit scale although it is the high speed of the number extremely smaller than the number of the analog value which should carry out A/D-conversion processing, concentration of much wiring to the large A/D converter of a circuit scale distributed in a three-dimension integrated circuit in this case from two or more analog values arises, and it is not desirable from a viewpoint of accumulation nature. Moreover, it means that the wiring distance from an analog value output part to an A/D converter becomes long, and the features of a three-dimension integrated circuit are not desirably harnessed from a viewpoint of S/N. Moreover, the technical problem of ** which that only the number equivalent to the number of each analog value is equipped with a flash plate mold A/D converter does not have from a viewpoint of a degree of integration, either exists. Moreover, naturally the fixed pattern noise should be removed and the device for it is also required for the analog value by which A/D conversion is carried out.

[0004]

[Means for Solving the Problem] In order to solve the above-mentioned technical problem the A/D converter of this invention The analog value are recording section which accumulates each analog data inputted from two or more analog data input terminal and two or more of these analog data input terminals, A digital counter and the D/A converter which changes the digitized output of this digital counter into an analog value, compared the output value and analog data of this D/A converter, and when a digital counter was a rise counter, the output value of a D/A converter exceeded the analog data -- or Two or more comparison means to distinguish that the output value of a D/A converter was less than the analog data when a digital counter is a down counter, It is the A/D converter equipped with the digital value are recording section which memorizes the digital value of a D/A converter in response to control by two or more of these comparison means, and has the scanning circuit which reads the output of the data of said digital value are recording section one by one further. Moreover, the sensor of this invention inputs the analog output of two or more sensing components into two or more analog data input terminals of the A/D converter of this invention. Furthermore, the three-dimension integrated circuit of this invention inputs into each analog data input terminal of the A/D converter of this invention each analog value distributed in a three-dimension integrated circuit. Moreover, in order to remove the fixed pattern noise of the analog value by which A/D conversion is carried out, the clamping circuit which consists of capacity and a switch for every analog data input terminal of the above-mentioned A/D converter is prepared.

[0005]

[Function] the are recording section which has an analog signal from two or more analog data input terminals according to an each individual by the configuration which described

this invention above -- accumulating -- this -- each of the comparator according to individual -- while transmitting to one input terminal, the analog value which the D/A converter which follows on the increment in the digital value of a counter, and increase or decrease in number gradually outputs is inputted into the input terminal of another side of said comparator in common as a reference value. When said reference value exceeds or is less than the analog value applied to one input terminal of said comparator, said each comparator output switches off to the timing based on the magnitude of said analog signal value for every comparator. Said switch connects the digital value of said counter which it has for every pixel to the digital value are recording section accumulated as an amount of binary for every bit. Therefore, when said switch is turned off based on the output of a comparator, the digital value corresponding to the amount of analog signals for every analog data input terminal is held at said digital value are recording section. Conversion to digital value from the above analog value is performed to juxtaposition about each analog data input terminal, and the time amount which this conversion takes is decided by count time amount of said counter based on a predetermined analog upper limit. If the conversion to digital value from the above-mentioned analog value is completed, the data of the aforementioned digital value are recording section will be outputted as digital value from a digitized output line one by one. By giving a lap by making the A/D-conversion time amount and digital signal output time amount for every analog data input terminal into timing, large A/D-conversion time amount can be taken with the increment in the number of analog input terminals. Moreover, by having prepared the clamping circuit for every analog data input terminal, by clamping the end which minded capacity to the timing in which the voltage output which bears at the time of **, i.e., light exposure, has appeared to the fixed electrical-potential-difference value, since the electrical potential difference of the difference of an output appears [in the output terminal which minded the capacity of said clamping circuit to the timing in which an output appears at the time of dark] at the time of an output and dark at the time of above **, a fixed pattern noise is removed.

[0006]

[Example] The example of this invention is explained below, referring to a drawing. Drawing 1 is the 1st example of the A/D converter of this invention. In drawing 1 , it has two or more analog data input terminals 1, and these data are held at the analog value are recording section 4 through the analog data transfer switch 3 driven with the analog value transfer gate terminal 2. 5 is a counter and is controlled by the counter clock input terminal 6 and the counter clear terminal 7. 8 is a binary output line from a counter 5. In addition, in drawing 1 , since it is easy, although the counter 5 is made into three bit counters, any bit counter is sufficient in fact. D/A converter 9 gives the data which changed the binary output from the binary output terminal 8 into the analog value to one input terminal of two or more comparators 10. The data held at said analog value are recording section 4 are inputted into the input terminal of another side of each comparator 10. In the comparative initial stage, the data of the analog value are recording section 4 are larger than the data of the analog output line of D/A converter 9, as for the output of a comparator 10, the 1st transfer switch 11 of digital data is made into an ON state, and the data of the binary output line 8 are transmitted to the 1st are recording section 12 of digital value as it is. If a counter 5 is a rise counter, when the data value of the analog output line of D/A converter 9 will exceed the data of the analog value are recording

section 4, for every analog juxtaposition input data, the 1st transfer switch 11 of digital data changes to an OFF state, and the data of the 1st are recording section 12 of digital data continue holding binary data just before the 1st transfer switch 11 of digital data changes to an OFF state henceforth. After a counter 5 finishes count-up to the maximum, the data of all the 1st are recording sections 12 of digital data are held through the 2nd transfer switch 14 of digital data at the 2nd are recording section 15 of digital value all at once with the digital value transfer gate terminal 13. The binary data held at the digital value are recording section 15 of the following 2nd are read to the digital signal output line 18 one by one as digital value for every analog juxtaposition input data through the digital data read-out switch 17 based on the juxtaposition output of a scanning circuit 16. As for a scanning circuit clock input terminal and 20, 19 is [a scan start signal input terminal and 21] scanning circuit carry-pulse output terminals.

[0007] In parallel to the period to the digital signal output line 18 for every analog juxtaposition input data by this scanning circuit when read-out is performed one by one, conversion to digital value from the analog value of the data of one group which made the train inputted into a degree is performed to juxtaposition for every analog input data as mentioned above. The analog value reset switch 22 is a switch for resetting the analog value are recording section 4, and is controlled by the reset gate terminal 23. This analog value reset switch 22 is required when the impedance of the analog data input terminal 1 is large, and especially when a data input is performed to the analog data input terminal 1 through a buffer with a small output impedance etc., it is not required. Although prepared respectively independently, since the counter full scale at the time of the number of analog juxtaposition input data which should be scanned, and A/D conversion generally differs, the scanning circuit clock terminal 19 and the scan start signal input terminal 20 of the counter clock input terminal 6 and the counter clear terminal 7 are obvious [this]. Moreover, it is also possible to carry out the series connection of two or more A/D converters shown in drawing 1 , and to enable it to perform A/D conversion of more analog juxtaposition input data, and this is easily realizable if the scanning circuit carry output terminal 21 of the A/D converter of the preceding paragraph is received in the scan start signal input terminal 20 of the A/D converter of the next step one by one. Although the analog value are recording section 4 and the digital value are recording sections 12 and 15 are described as a capacitive component, this is good also as a register which also contained the impedance-conversion component further.

[0008] The digital value are recording section 15 and the 2nd transfer switch 14 of digital data are used as the flip-flop which uses the digital value transfer gate terminal 13 as an enabling terminal, and that of especially the digital value are recording section 12 and the 1st transfer switch 11 of digital data are good for the flip-flop which uses the gate terminal of the 1st transfer switch 11 of digital data as an enabling terminal also as a static register. D/A converters 9 are common D/A converters, such as a weighting mold and R-2 R form. Moreover, although an A/D converter as shown in this Fig. enters under the category of the A/D converter called an integral mold and a counter mold and explained as a count-up mold in the above-mentioned explanation, it is good also as a count-down mold. In the case of a count-down mold, in a comparative initial stage, the data of the analog value are recording section 4 are smaller than the data of the analog output line of D/A converter 9. Although the output of a comparator 10 makes an ON state the 1st transfer switch 11 of digital data and the data of the binary output line 8 are

transmitted to the 1st are recording section 12 of digital value as it is When the data value of the analog output line of D/A converter 9 is less than the data of the analog value are recording section 4, the 1st transfer switch 11 of digital data changes to an OFF state for every analog juxtaposition input data. The data of the 1st are recording section 12 of digital data will continue holding binary data just before the 1st transfer switch 11 of digital data changes to an OFF state henceforth.

[0009] When considering as an A/D converter only with one configuration shown in drawing 1 , common connection is possible for the scan start signal input terminal 20 and the counter clear terminal 7, and if a counter full scale and the number of analog juxtaposition input data are still more nearly equal, it is also possible to use them, carrying out common connection of the scanning circuit clock input terminal 19 and the counter clock input terminal 6. One example of the timing chart for driving the A/D converter of drawing 1 to drawing 2 is shown. In drawing 2 , it is supposed that the scan output period of the digitized data is longer than an A/D-conversion period. In order that an A/D-conversion period and a digitization data output period may carry out synchronization, the interval which can give analog juxtaposition input data is decided by the period of the longer one of these both. Moreover, in order for an A/D-conversion period and a digitization data output period to carry out synchronization, H level period of a digital value transfer gate terminal must expire early rather than a digitization data output period begins. (-- the analog juxtaposition input signal reset signal in drawing 2 is a thing in the case of resetting the source of data of the analog data input terminal 1 of drawing 1 , and it touches in explanation of the example of the sensor of below-mentioned this invention.) -- since the data which appear in the digital signal output line 18 in time are binary data, high-speed read-out is possible for them one by one for every analog juxtaposition input data. While this read-out is performed, conversion to digital data from analog data is performed to juxtaposition coincidence in each analog juxtaposition input data. The number of analog juxtaposition input data is 2500 temporarily, and if this is read from the digital signal output line 18 by 5MHz with the resolution of 8 bits, the read-out period for 500 microseconds is needed. 1 clock period has been about 2 microseconds since the binary output line 8 and the digital signal output line 18 become eight and the full scale should count only 255 clocks in said 500 microseconds by 8 bits, if a counter 5 was 255. Therefore, since the operational amplifier of a low slew rate can be used as an internal component of D/A converter 9 possible [the A/D conversion which is generous in time] therefore, there is also no bad influence of a glitch and highly-precise-izing is possible. Although considered as the A/D converter of a triplet by this example again, it is in ** that it is easily extensible to the A/D converter of the number of bits of arbitration.

[0010] Furthermore, although the analog data transfer switch 3, the 1st transfer switch 11 of digital data, the 2nd transfer switch 14 of digital data, the digital data read-out switch 17, and the reset switch 22 have given depiction and explanation as N-channel metal oxide semiconductor FET respectively in drawing 2 , not N-channel metal oxide semiconductor FET but P channel MOSFET, a juxtaposition CMOS switch, or JFET may be used. When taking into consideration further the effect to the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switch, a juxtaposition CMOS switch is desirable.

[0011] Drawing 3 omits the digital value transfer gate terminal 13 and the 2nd transfer

switch 14 of digital data in drawing 1 , and is the 2nd example of the A/D converter of this invention. Since the thing of a number equal to the component used into drawing 1 with the component in drawing 3 is functionally equal, it omits explanation. 24 in drawing 3 is the digital value are recording section.

[0012] The timing chart for the drive of drawing 3 becomes like drawing 4 . That is, a **** A/D-conversion period appears in the inside of the interval to which an analog parallel input is given, and a digitization data output period appears succeedingly. That is, since an A/D-conversion period and a digitization data output period do not lap in time, the 2nd transfer switch of digital data is omissible. The configuration of such an A/D converter has the effective full scale of the digitized output of an A/D converter, when very small as compared with the amount of analog data by which a parallel input is carried out at once. For example, although the time amount which 5MHz read-out takes to the number of parallel inputs 5000 is 1 m seconds, the A/D-conversion period which set the full scale of a digitized output to 7, and set the counter clock to 100kHz becomes about 70 microseconds, and is understood that this A/D converter is very small effective compared with 1 m seconds.

[0013] The series connection of the more than one is carried out like the A/D converter shown in drawing 1 , and the A/D converter shown in drawing 3 can also be enabled it to perform A/D conversion of more analog juxtaposition input data. Although the analog value are recording section 4 and the digital value are recording section 24 are described as a capacitive component, this is good also as a register which also contained the impedance-conversion component further. Especially the digital value are recording section 24 and the digital data transfer switch 11 are used as the flip-flop which uses the gate terminal of the digital data transfer switch 11 as an enabling terminal, and are good also as a static register. Moreover, it is good as any of a count-up mold or a count-down mold as well as the A/D converter which also showed this A/D converter to drawing 1 . Since an A/D-conversion period can use the operational amplifier of a low slew rate as well as the A/D converter of drawing 1 as an internal component of D/A converter 9 also in this A/D converter when sufficiently small compared with a digital data output period, the bad influence of a glitch can be reduced. Although this example was also used as the A/D converter of a triplet again, it is in ** that it is easily extensible to the A/D converter of the number of bits of arbitration. Furthermore, although the analog data transfer switch 3, the digital data transfer switch 11, the digital data read-out switch 17, and the reset switch 22 have given depiction and explanation as N-channel metal oxide semiconductor FET respectively also in drawing 4 , not N-channel metal oxide semiconductor FET but P channel MOSFET, a juxtaposition CMOS switch, or JFET may be used. When taking into consideration further the effect to the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switch, a juxtaposition CMOS switch is desirable.

[0014] The 1st and 2nd examples of the sensor of this invention are shown in drawing 5 and drawing 6 . Drawing 5 and drawing 6 add the sensing component 25 to each of the analog data input terminal of the shape of an array of the A/D converter respectively shown in drawing 1 and drawing 3 . If each sensing component 25 accepts the part and need which act as transformer Duce of the physical quantity which should be detected to an electrical potential difference in drawing 5 and drawing 6 , the reset switch and buffer output circuit which initialize the detecting element itself are also included. (The timing

chart of the reset switch described here of operation shows drawing 2 and drawing 4 as an analog juxtaposition input signal reset signal.) For example, if the signal in the detecting element in the sensing component 25 is an output gestalt as a current, each sensing component 25 contains a current / electrical-potential-difference conversion circuit. The sensor shown in drawing 5 leads the output of each sensing component 25 to the analog data input terminal 1 of the A/D converter shown in drawing 1 at juxtaposition, and the following actuation is as the timing chart shown in drawing 2 . Moreover, the same is said of the sensor shown in drawing 6 , the output of each sensing component 25 is led to the analog data input terminal 1 of the A/D converter shown in drawing 3 at juxtaposition, and the following actuation is as the timing chart shown in drawing 4 . By the sensor of such a configuration, it is possible to consider as 1 chip integration device or a hybrid integration device also including an A/D converter, and not causing deterioration of a signal quality is mentioned as a description that it can digitize without degrading, the precision, i.e., S/N, of analog data, and by pulling out an output signal as digital data out of said device.

[0015] Although the one dimensional array-like sensor was explained in drawing 5 and drawing 6 , a two-dimensional-array-like sensor is further explained using drawing 7 . 26 in drawing 7 is the area sensing component of a M line N train, M steps of vertical-scanning circuits and 28 are the sensing component output terminals for every train of N individual, the sensing component of a MxN individual and 27 connect this sensing component output terminal 28 to the analog data input terminal 1 of the A/D converter respectively shown in drawing 1 or drawing 3 , and drive the scanning circuit 16 of an A/D converter as a horizontal scanning circuit, and 25 constitutes a two-dimensional-array-like sensor. It drives so that the A/D conversion and the digital scan output of data of one line may be obtained for one step of every perpendicular transfer.

[0016] By the sensor of such a configuration, it is possible to consider as 1 chip integration device or a hybrid integration device also including an A/D converter, and deterioration of a signal quality is not caused that it can digitize without degrading, the precision, i.e., S/N, of analog data, and by pulling out an output signal as digital data out of said device.

[0017] Drawing 8 shows the area sensor of the 1st more concrete example at the time of the sensor of drawing 7 being based on a CCD sensor. 31 is the A/D converter shown in drawing 1 or drawing 3 . In drawing 8 , after the charge stored in each photodiode 39 according to incidence light exposure is transmitted to the perpendicular charge transfer way 41 by the drive of the transfer gate 40 for every perpendicular blanking period, the perpendicular charge transfer way 41 is perpendicularly transmitted one by one by driving the clock pulse terminal 42. Henceforth, the charge of each train is transmitted to the suspension diffusion field 34 by the drive of the output gate 35 for every line for every level blanking period. Said suspension diffusion field 34 detects to coincidence the analog value which functions as suspension diffusion mold amplifier and each charge in the suspension diffusion field 34 has with a buffer 33, and inputs this into the analog data input terminal 1 of A/D converter 31 respectively. Below, for every line, A/D conversion of the analog data of each train is carried out to juxtaposition, and it is serially outputted to the digital signal output line 18 as digital value. It is for resetting by connecting the diffusion field 38 which a reset gate 36 drives this and is in reset potential, and said suspension diffusion field 34 into drawing 8 . 37 is Rhine for maintaining the potential of

the diffusion field 38 at reset potential. 1, 18, 19, and 20 are respectively equal to the thing of the same number in drawing 1 or drawing 3 .
[0018] In addition, although explained as a sensor which has an A/D-conversion function based on the charge transfer mold image sensor of an INTARAIN transfer mold in drawing 8 , the sensor which has an A/D-conversion function similarly to the charge transfer mold image sensor of a frame transfer mold or a frame INTARAIN transfer mold is realizable.
[0019] By the way, since this serves as a fixed pattern noise when it has the offset value from which the analog value given to two or more analog data input terminals differs for every analog data input terminal, before carrying out A/D conversion of this, it is necessary to remove. Therefore, if the clamping circuit which consists of capacity, a switch, etc. for every analog data input terminal is prepared, a fixed pattern noise is removable.
[0020] Therefore, in the sensor of drawing 8 , it is good also as a thing including the correlation duplex sampling circuit which considers the clamping circuit which consists a buffer 33 of capacity and a switch in order to reduce a noise as a basic configuration. That is, by clamping the output terminal of the clamping circuit of each train on the fixed electrical potential difference immediately after keeping simultaneous the suspension diffusion fields 34 of each train to reset potential about each level blanking period, when the output which bear light exposure all at once to the suspension diffusion field 34 of each of said train appears, to the output terminal of the clamping circuit of each of said train, the output from which the fixed pattern noise was removed is obtained. In order to carry out A/D conversion for every train by this, suitable analog output is obtained.
[0021] Drawing 9 (a) shows the area sensor of the 2nd more concrete example at the time of the sensor of drawing 7 being based on a magnification mold MOS sensor. The A/D converter which showed 31 to drawing 1 or drawing 3 , the component in which 47 forms a constant current source, and 1, 18, 19 and 20 are equals respectively at drawing 1 or the same number thing of drawing 3 . In drawing 9 (a), the transfer switches 43 turn on the charge stored in each photodiode 44 according to incidence light exposure all at once for every level blanking period about the line chosen by work of a vertical-scanning circuit, and it is stored as gate potential of the transistor 45 for magnification. This later transfer switch 43 is made into an OFF state. By making the drain of the transistor 45 for magnification high-level at this time, it appears in the perpendicular output line 46 whose follower output based on the gate potential of the transistor 45 for magnification of one line by which current selection is made is the common source of the transistor 45 for magnification. When the output of one certain line appears in the perpendicular output line 46, the follower output of the above-mentioned gate potential after the follower output which bears the light exposure information on the line first appeared and continued and the gate potential of the transistor 45 for magnification of the line was reset by the predetermined reset value with the transistor 49 for reset appears. By this sensor, property dispersion on the manufacture to the threshold voltage of the transistor 45 for magnification arises for every pixel, and this appears as follower output dispersion, i.e., a fixed pattern noise, even if the gate potential of the transistor for magnification is set as constant value. Therefore, it is required to take the difference of the follower output which bears the above-mentioned light exposure information, and the follower output after reset. This approach is explained below. When the follower output which bears the

aforementioned light exposure information has appeared in the perpendicular output line 46, the reset switch 48 which resets the potential of the terminal 51 by the side of the buffer 52 of the joint capacity 50 is turned ON. Next, after the reset switch 48 of the potential of a terminal 51 turns off, the follower output of the gate potential which turns ON the transistor 49 for gate potential reset of the transistor 45 for magnification, and is in the perpendicular output line 46 shortly at reset potential appears. At this time, the electrical potential difference of the difference of the follower output of the gate potential in said reset potential and the follower output which bore said light exposure information appears in a terminal 51, and this is respectively inputted into the analog data input terminal 1 of A/D converter 31 for the output voltage of this difference for every train through a buffer 52. The fixed pattern noise resulting from property dispersion of each transistor for magnification is removed by taking difference as mentioned above. Below, A/D conversion of the analog output of the difference of each train is carried out to juxtaposition, and it is serially outputted to the digital signal output line 18 as digital value. Hereafter, for every level blanking period, if the analog output of the difference of each train is inputted into said A/D converter 31 at juxtaposition, it is serially changed and outputted one line at a time to digital value. In addition, an amplifier may be inserted between the perpendicular signal line 46 and a terminal 51, and when this amplifier consists of a buffer stage which follows the voltage amplification section and it, a large output signal can be taken. the difference of the above [immediately after / this] -- since there is a circuit which takes an electrical potential difference, a fixed pattern noise is removed too.

[0022] Since the approach for removing the fixed pattern noise used by the sensor of drawing 9 (a) works effectively also as a sensor which does not have an A/D-conversion function, such a case is explained using drawing 9 (b). The transfer switches 43 turn on the charge stored in each photodiode 44 according to incidence light exposure all at once for every level blanking period about the line chosen by work of a vertical-scanning circuit, and it is stored as gate potential of the transistor 45 for magnification. This later transfer switch 43 is made into an OFF state. Although the follower output which bears light exposure information at this time has appeared in the perpendicular output line 46, the reset switch 48 which resets the potential of the terminal 51 of the joint capacity 50 here is turned ON. Next, after the reset switch 48 of the potential of a terminal 51 turns off, the follower output of the gate potential which turns ON the transistor 49 for gate potential reset of the transistor 45 for magnification, and is in the perpendicular output line 46 shortly at reset potential appears. At this time, the electrical potential difference of the difference of the follower output of the gate potential in said reset potential and the follower output which bore said light exposure information appears in a terminal 51. Amplifier 86 may be inserted between the perpendicular signal line 46 and the joint capacity 50. the case where amplifier 86 has a voltage amplification function -- an output signal -- large -- it can take -- also in this case -- the time of ** -- the time of an output and dark -- the difference during an output -- since the circuit which takes an electrical potential difference is prepared, a fixed pattern noise is removable too. the time of ** which appeared in the terminal 51 -- the time of an output and dark -- difference with an output -- an electrical-potential-difference value is outputted to the common water Hiraide line of force 85 through the sequential switch 84 by the output pulse of a horizontal scanning circuit. The heterogeneity of the exposure time for every train that an

output becomes large must have been produced, so that the charge by exposure of this horizontal scanning period becomes the train read later with the gate of the transistor 45 for magnification since it dissociates since the transfer switch 43 is turned off.
[0023] It makes it possible to carry out without being able to obtain the analog data from which the suitable fixed pattern noise for A/D-conversion processing was removed, and the inside of the same chip as a sensor or the location which approached taking a long time for digitization of the analog quantity of a sensing component at a conversion time according to the sensor of this invention, above, and the data collection of high quality becomes possible extremely at a high speed. Since this invention has big effectiveness also in a hybrid configuration, combination is possible for the sensing component for which a material differs from the semi-conductor used for the A/D converter, and it can say that the applicability is very wide.
[0024] In addition, this invention is applicable also in the sensing component treating other physical quantity which made the shape not only of optical information but an array, although the image sensors which treat optical information as a sensor in explanation of the application to a sensor were taken up.
[0025] Next, the example of the three-dimension integrated circuit of this invention is explained, referring to a drawing. Drawing 10 is the three-dimension integrated circuit of the example of this invention. It consists of the 1st layer, the 2nd layer, and the 3rd layer in drawing 10 . The 1st layer is a photo-electric-conversion layer, and consists of a photo-electric-conversion unit element child of five-line five trains in drawing 10 . The 2nd layer is an A/D-conversion layer, and as shown in drawing 10 , it consists of an A/D-conversion unit element child of five-line five trains corresponding to the optoelectric transducer of the 1st layer. The 3rd layer is a data-processing layer. What formed the signal transfer section, the storage section, the power supply section, the mechanical component, etc. for every layer further as a three-dimension integrated circuit exists, and, generally all have much the inputs or the generating sections, and the A/D-conversion sections of analog data used as the photo-electric-conversion section in drawing 10 . Although a layer [2nd] A/D-conversion layer has the function to change many analog values into the digital value of a same number individual, it doubles the A/D-conversion unit component section and the A/D-conversion common section for the A/D-conversion layer, and shows them to drawing 11 . In drawing 11 , the A/D-conversion unit component section is drawn as a form located in a line in the shape of [of two line two trains] an array. This A/D-conversion layer is equivalent to what arranged what does not take into consideration the serial output method of a digital value output in the A/D converter of drawing 1 which is the already explained example, and drawing 2 in the shape of a two-dimensional matrix. That is, it is the A/D converter of the parallel input of two or more data, and a parallel output. It has two or more analog data input terminals 61 which should receive an analog quantity from the photo-electric-conversion layer of drawing 10 in drawing 11 , and these data are held at the analog value are recording section 64 through the analog data transfer switch 63 driven with the analog value transfer gate terminal 62. 65 is a counter and is controlled by the counter clock input terminal 66 and the counter clear terminal 67. 68 is a binary output line from a counter 65. In addition, in drawing 10 , since it is easy, although the counter 65 is made into three bit counters, according to the gradation nature for which it asks theoretically, any bit counter is sufficient. D/A converter 69 gives the data which changed the binary output from the

binary output terminal 68 of a counter 65 into the analog value to one input terminal of two or more comparators 70 through the D/A-converter analog output line 74. The data held at said analog value are recording section 64 are inputted into the input terminal of another side of each comparator 70. In the comparative initial stage, the data of the analog value are recording section 64 are larger than the data of the analog output line of D/A converter 69, as for the output of a comparator 70, the digital data transfer switch 71 is made into an ON state, and the data of the binary output line 68 are transmitted to the digital value output terminal group 75 through the buffer amplifier 72. If a counter 65 is a rise counter, when the value of the analog output line 74 of D/A converter 69 will exceed the data of the analog value are recording section 64, the digital data transfer switch 71 changes to an OFF state for every analog juxtaposition input data to the timing which became independent for each photo-electric-conversion unit element child of every, and the data of the digital value are recording section 77 and a buffer amplifier 72 continue holding binary data just before the digital data transfer switch 71 changes to an OFF state henceforth. After a counter 65 finishes counting up to the maximum, illustration is not carried out, but if it is made the configuration which samples the digital value output of each digital value output terminal group 75, the digital value equivalent to the analog value given to each analog parallel data input terminal 61 will be obtained for every input terminal. The digital value obtained for every pixel below is transmitted to the data-processing layer of drawing 10 , and an image processing is performed. The analog value reset switch 76 is a switch for resetting the analog value are recording section 64, and is controlled by the reset gate terminal 73. This analog value reset switch 76 is required when the impedance of the analog data input terminal 61 is large, and especially when a data input is performed to the analog data input terminal 61 through a buffer with a small output impedance etc., it is not required. Although the analog value are recording section 64 and the digital value are recording section 77 are described as a capacitive component, this is good also as a register which also contained the impedance-conversion component further.

[0026] Especially the digital value are recording section 77 and the digital data transfer switch 71 are used as the flip-flop which uses the gate terminal of the digital data transfer switch 71 as an enabling terminal, and are good also as a static register. D/A converters 69 are common D/A converters, such as a weighting mold and R-2 R form. Moreover, although an A/D converter as shown in this Fig. enters under the category of the A/D converter called an integral mold and a counter mold and explained as a count-up mold in the above-mentioned explanation, it is good also as a count-down mold. In the case of a count-down mold, in a comparative initial stage, the data of the analog value are recording section 64 are smaller than the data of the analog output line 74 of D/A converter 69. Although the output of a comparator 70 makes the digital data transfer switch 71 an ON state and the data of the binary output line 68 are transmitted to the digital value are recording section 77 as it is When the data value of the analog output line 74 of D/A converter 69 is less than the data of the analog value are recording section 64, the digital data transfer switch 71 changes to an OFF state for every analog juxtaposition input data. The data of the digital value are recording section 77 will continue holding binary data just before the digital data transfer switch 71 changes to an OFF state henceforth. By the way, the data which appear in the digital value output terminal group 75 can be read all at once for every analog juxtaposition input data. This

is conditions desirable as an A/D converter of a three-dimension integrated circuit. Moreover, the A/D-conversion element number per photo-electric-conversion unit element child is smaller than the A/D converter of the usual flash plate mold. It is because this consists of a device of the structure with it for a component required as an A/D-conversion unit element child about per photo-electric-conversion unit element child. [there is also little number, such as a comparator, the digital data are recording section, a digital data transfer switch, the analog data are recording section, an analog data transfer switch, a reset switch, and a buffer amplifier, and very simple] Although the digitized output of this 11 Fig. is made into the triplet in order to illustrate simply, if the juxtaposition number of the binary output line 68, the digital data transfer switch 71, and a buffer amplifier 72 is made into eight, a 8-bit digitized output is easily realizable. Conversion to digital data from analog data is performed to juxtaposition coincidence in each analog juxtaposition input data. if the full scale of a counter 65 is 255, even if it is a frame period short for about 500 microseconds that what is necessary is to count only 255 clocks within a frame period -- a maximum of -- the A/D conversion of about 500kHz which may drive with the clock of low frequency comparatively, therefore is generous in time is possible, since the operational amplifier of a low slew rate can be used as an internal component of D/A converter 69, there is also no bad influence of a glitch and highly-precise-izing is possible. Therefore, although the A/D converter of a flash plate mold is not high-speed, if it carries out from the frame frequency of the usual optoelectric transducer, a high speed and highly precise A/D conversion are fully made, and the three-dimension integrated circuit of high performance can be realized extremely. Although considered as the A/D converter of a triplet by this example again, it is in ** that it is easily extensible to the A/D converter of the number of bits of arbitration.

[0027] Furthermore, although the analog data transfer switch 63, the digital data transfer switch 71, and the reset switch 76 have given depiction and explanation as N-channel metal oxide semiconductor FET respectively in drawing 11 , not N-channel metal oxide semiconductor FET but P channel MOSFET, a juxtaposition CMOS switch, or JFET may be used. When taking into consideration further the effect to the data (especially analog data) of the feed-through potential fluctuation by the gate potential change at the time of driving a switch, a juxtaposition CMOS switch is desirable.

[0028] What is necessary is just to give the potential of the other-end child who bears light exposure information to the analog data input terminal 61 in drawing 11 , when terminal potential of one of these is fixed that the electrical potential difference between the terminal should just be what changes according to light exposure as a photo-electric-conversion unit element child in the photo-electric-conversion layer of drawing 10 . For example, what is necessary is just to give the potential difference between the terminal to the analog data input terminal 61 of drawing 11 using a photodiode. A photo-electric-conversion unit element child for drawing 12 to improve the charge capacity over the analog value are recording section in drawing 11 is shown, 78 is a photo-electric-conversion basic device represented by the photodiode etc., and connection is carried out to the gate terminal of the impedance-conversion component 79 which takes follower circuitry for the terminal of one of these to carry out impedance conversion of another side at a fixed potential edge, and raise the current drive capacity as a photo-electric-conversion unit element child. 80 is a reset switch for resetting the potential difference between the both-ends children of the photo-electric-conversion ingredient 78. It is used

giving the electrical-potential-difference value which appears in the source terminal 81 of the impedance-conversion component 79 to the analog data input terminal 61 of drawing 11 .

[0029] As mentioned above, according to the above configurations, it is possible to form a high-speed highly precise A/D converter for every unit optoelectric transducer with easy circuitry and a small element number, and the three-dimension integrated circuit of a high degree of integration in which high precision digital signal processing is possible can be realized.

[0030] In addition, although the optoelectric transducer was made into the analog data input source, this invention can be applied when the sensing device treating other physical quantity other than the light which made the shape not only of optical information but an array is made into an analog data input source. Furthermore, even if especially the input source of said analog data does not need to be an output from a sensing device and it is a certain analog value which appeared in process of signal processing, it is satisfactory and this invention is essentially applied. Moreover, if a clamping circuit is prepared as drawing 9 (a) and (b) explained, if required, it is possible to also realize the three-dimension integrated circuit which has the removal function of a fixed pattern noise.

[0031]

[Effect of the Invention] If it becomes possible to save an A/D-conversion period to digital value, and to change two or more analog values by which a parallel input is carried out with high precision by easy circuitry, while the sensor which has the removal function of a fixed pattern noise becomes possible according to this invention as explained above, the A/D converter of high-speed highly precise parallel input / serial output is realizable things and by carrying out rapid scanning of the changed digital value, and outputting it. Moreover, by adding the sensing component of the shape of an array which gives the analog data which should be inputted into the above-mentioned A/D converter, it can become possible to change the analog value based on various kinds of physical quantity amount of information of a sensing component into juxtaposition for every sensing component at digital value, said digital quantity can be read to a high speed, and a high speed and the array-like sensor of high S/N can be realized. For example, if light is treated as said physical quantity, this invention is very useful as a picture input device. Furthermore, if the A/D-conversion layer which considers the above-mentioned A/D converter as a multi-input multi-output configuration, and carries out A/D conversion of many analog values by this is formed, it is highly precise and the three-dimension integrated circuit which is a high degree of integration can be realized. This invention is especially very suitable in the object for three-dimension integrated-circuit division image processings for three-dimension integrated circuits which has an array-like sensing component.

[0032] As explained above, the effectiveness on the industry of this invention is size very much.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The circuit diagram in the 1st example of the A/D converter of this invention
[Drawing 2] The drive timing chart of the A/D converter of drawing 1
[Drawing 3] The circuit diagram in the 2nd example of the A/D converter of this invention
[Drawing 4] The drive timing chart of the A/D converter of drawing 3
[Drawing 5] The circuit diagram in the 1st example of the sensor of this invention
[Drawing 6] The circuit diagram in the 2nd example of the sensor of this invention
[Drawing 7] The block diagram of a two-dimensional-array-like sensor
[Drawing 8] The block diagram of the sensor of the shape of a two dimensional array of the 1st example of this invention
[Drawing 9] For the block diagram (b) of the sensor of the shape of a two dimensional array of the 2nd example of this invention, (a) is the block diagram of the sensor of the shape of a two dimensional array which is not equipped with an A/D-conversion function.
[Drawing 10] The functional description Fig. of the three-dimension integrated circuit of the example of this invention
[Drawing 11] The circuit diagram of the A/D converter used for the three-dimension integrated circuit of this invention
[Drawing 12] A photo-electric-conversion unit element child's circuit diagram
[Description of Notations]
1 Analog Data Input Terminal
4 Analog Value Are Recording Section
5 Counter
9 D/A Converter
10 Comparator
11 1st Transfer Switch of Digital Data
12, 15, 24 Digital value are recording section
13 Digital Value Transfer Gate Terminal
14 2nd Transfer Switch of Digital Data
16 Scanning Circuit
25 Sensing Component
31 Parallel in-Serial Out A/D Converter
34 Suspension Diffusion Field
39 Photodiode
40 Transfer Gate
41 Perpendicular Charge Transfer Way
44 Photodiode
45 Transistor for Magnification
46 Perpendicular Signal Line
50 Joint Capacity
51 Differential Signal Output Terminal
61 Analog Data Input Terminal
63 Analog Data Transfer Switch
65 Counter
69 D/A Converter

70 Comparator
71 Digital Data Transfer Switch